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Optimizing Power Consumption in IoT Wearable Devices Using VLSI

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Abstract— **Management of power consumption in IoT wearable devices through Very Large-Scale Integration (VLSI) is vital in augmenting the capability of these devices, their battery life as well as the total experience that a user has with the device. Due to continuous advances in wearable technology, power consumption management is a concern in order to reach a proper balance between performance and energy. Several approaches concerning VLSI architectures in a smart power management of portable applications are also discussed in this paper, VLSI which includes low power design methodologies, dynamic power management, ultra-low power modes and the use of custom ASICs. Formulated for expert-level, it also covers general ideas such as energy harvester technologies, SoC integration of power management blocks, low power communication protocols, and using advanced semiconductor processes to minimize power usage. thermal control along with the techniques of low power memory technologies show that VLSI has the ability to make wearable devices perform in balance with low power consumption which can make the wearable devices last longer, more reliable and practical for use. These innovations are critical to address the issues of power dominance of wearable devices and guaranteeing future enhancement of wearables in various applications.**

***Index Terms*—IoT Wearable Devices, VLSI, Power Optimization, Low-Power Design, Dynamic Power Management (DPM), Ultra-Low-Power Modes, Custom ASICs, Energy Harvesting, System-On-Chip (SoC), Power-Efficient Communication, Thermal Management, Low-Power Memory Technologies.**

I. INTRODUCTION

The paper "Optimizing Power Consumption in IoT Wearable Devices Using VLSI" discusses using VLSI to design and implement circuits that minimize power consumption in IoT wearable applications. The increased complexity of wearable technology and the desire to continue powering the modest battery within the wearable and prevent the need for any additional heating makes managing power a key fundamental concern. Smart jewelry, smart watches, fitness, trackers, and health monitoring wearables are becoming far more commonplace giving the user real-time data and ease of use. Nevertheless, these devices can be operated with limited energy, with a small battery pack being usually used hence; power control is mandatory. Wearables need to function for extended periods without human intervention so there is constant pressure for value to be added to the tech without sacrificing comfort. This challenge is met through the use of VLSI to integrate millions of transistors into a single circuit, thus resulting in compact, low-power circuits.

Power management in IoT wearables can be achieved by using the following power-aware techniques in VLSI-based solutions. An example is Dynamic Voltage and Frequency Scaling (DVFS) where the device works at different voltage levels according to the load density hence avoiding wastage of energy power levels. Power gating and sleep modes also allow a device or component to be switched off or put into a very low power mode where they are not needed. Further, reduced power consumption abilities in application-specific integrated circuits (ASICs) are incorporated into wearable technologies for applications like biometric monitoring with optimization of efficiency.

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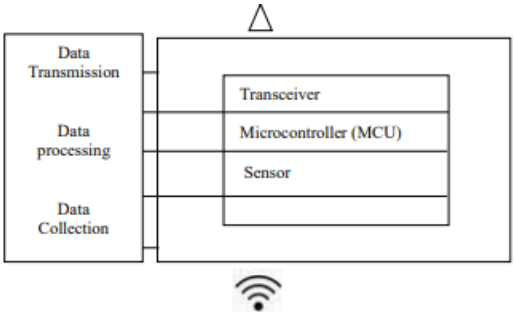

Fig.1: The Essential Components Things (IoT) Enabled Smart Sensing Device [21]

The other area that needs considerable efficiency is communication. IoT wearables depend on connectivity and VLSI designs consist of power-efficient electronic communication techniques such as BLE or Zigbee. These protocols reduce power consumption during data transmission which is essential in order to have a longer lifespan of wearables. Energy harvesting microcircuits used in the contemporary VLSI wearables' design harvest energy from specific sources such as heat, motion, or light to be converted into electricity. Battery life is also conserved by using this supplement to minimize the number of charges needed.

Also, innovative technologies such as FinFET and ultra-low power CMOS technologies enabled on chip the reduction of power leakage, thereby enhancing the energy efficiency of IoT wearable devices. In conclusion, this paper reveals that the specific problem of high power consumption in IoT wearables can be effectively addressed through the enhancement of VLSI technology. This guarantees that with the help of the attained high design techniques wearable devices can provide improved performance, battery life, as well as user experiences.

II. Low-Power Design Techniques

Thus, in conjunction with the emerging management of overall power utilization for IoT wearable devices based on VLSI, the principles of low-power design are of significant importance. Smart wristbands, activity trackers, and smartwatches should constantly function as watches, although battery volume is limited; thus, energy efficiency is crucial. VLSI design allows controlling power consumption on the circuit level to a very high extent through several novelties designed to minimize both dynamic and static power losses.

That is why dynamic power, also referred to as switching power, is the energy consumed by a transistor in its switching between states 0 and 1. The most competitive approach is to decrease the supply voltage which in turn will decrease the dynamic power consumption [1]. The amount of dissipated power is proportional to the square of the supply voltage; therefore decreasing the voltage a little will result in a lot of power saved. However, this has to be achieved most appropriately so that the performance of the devices is not affected.

Another of these techniques is the sizing of the transistors to optimize their usage. Since the size of the transistors is a critical factor in the performance of these circuits and the power dissipated in them, size is an important consideration in VLSI design. Faster switching transistors mean that the current must be controlled and must use less energy which leads to concerns over leakage power when using smaller transistors than the reference. Quiescent power or Standby power is the amount of energy consumed by any transistor that is on but does not change its state regularly. For IoT wearables, which are typically in low-/ no-usage –mode for much of the time, leakage is especially detrimental to battery life.

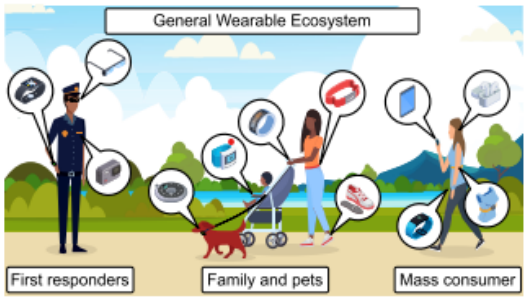

Fig.2: Forthcoming wearable integration scenario [3]

For that purpose, new approaches like multi-threshold voltage (multi-Vt) design are employed. This approach provides the capability that different transistors of a common type can employ different threshold voltages. The low-threshold voltage transistors are used where high-speed performance is essential in contrast with high-threshold voltage transistors used where leakage current is a more significant concern [2].

Moreover, dynamic power is managed using clock gating to switch the clock signal to parts of the circuit that are not active, thereby avoiding unnecessary usage of the circuit.

In general, all these low-power design techniques are major building blocks to enhancing the battery life of IoT wearables and their overall efficiency making them more user-friendly.

III. Dynamic Power Management (DPM)

Ergo, Dynamic Power Management (DPM) is perhaps one of the most important approaches to power management within IoT wearable devices, much more so in the case where VLSI is employed. Smartwatches and fitness trackers are designed to operate while interacting with users and their surroundings, however, the amount of interaction they have with their surroundings constantly changes during the day. DPM also enables these devices to dynamically manage the power Submit your manuscript electronically for review.

consumption in direct proportion to the operational demand, therefore optimizing battery longevity as well as the related performance.

Among all the DPM techniques, Dynamic Voltage and Frequency Scaling (DVFS) is one of the most used techniques. DVFS enables the wearable device to control the supply voltage and the clock based on the level of processing of the system [3]. For instance, when the device is idle, which entails the display of just the time or monitoring mild motion, this can lower both its voltage and frequency to very low levels. On the other hand, when this comes to the instance where the device has to perform more complex activities like a fitness application, or when this has to transfer data to a smartphone, this can raise the voltage and frequency for efficient tasking. Dynamic voltage and frequency scaling means that both, voltage and frequency are varied so that wearables can achieve the targeted longevity of battery life, without the necessity of compromising the interactivity and response time of the smart device.

Besides DVFS, there are other hooks for DPM strategies, for instance, power gating where subsets of the device's circuitry are switched off where unneeded. For example, as witnessed when the wearable is inactive, in its sleep state, or most of the time, non-papers in the wearable can be shut down completely hence eliminating a significant amount of power consumption [4]. This selective deactivation of circuitry makes the wearables stay functional for quite a long time without requiring frequent charging.

DPM techniques prove useful in IoT wearables because these devices are usually worn perpetually, thereby requiring the user to go for days before recharging the wearables. With DPM using VLSI, manufacturers can minimize power consumption during active idle time when this is most important that the device is on and immediately responsive while using the least power.

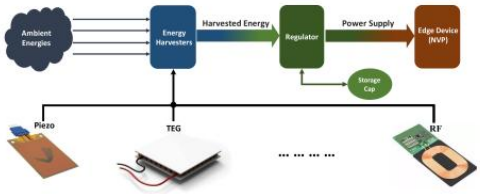

Fig.3: System architecture of self-powered non-volatile IoT edge device.[22]

Therefore, Dynamic Power Management is effective in improving energy efficiency in IoT wearable devices since this will increase the battery life, the scalability of the performance, and user satisfaction.

IV.Custom Application Specific Integrated Circuits (ASICs)

Application Specific Integrated Circuits (ASICs) are specific circuits developed for selected particular uses, and they play a crucial role given their efficiency when this comes to power controls for IoT wearables. Therefore, custom ASICs for wearables differ from general-purpose processors providing a variety of functions that are designed for fitness tracking, health monitoring, or biometric data processing [5]. This specialization facilitates the ASICs to work with significantly lower power, faster, and with less space compared to any other general-purpose microprocessor.

Smart and wireless wearable devices such as fitness trackers, smartwatches, and medical sensors are always needed to monitor and analyze data continuously, usually under

constrained power budgets. What custom ASICs offer the designer is the ability to focus on these specific jobs and allow the device to do its work with a minimal amount of energy expenditure. For example, an ASIC dedicated just to heart rate monitor will support only the essential components needed for that task, no extra power will be consumed for operations that are required in ordinary microcontrollers for other purposes.

Getting efficiency from power in custom ASICs is possible since they are designed with fewer transistors and less complex circuitry included in their creation. This results in both higher dynamic power dissipation (the power utilized when the device in question is processing info) and static power or leakage power (the power that is utilized by the transistors when they are off). Moreover, there can be separate ways of reducing power consumption within ASICs for example: During low activity, ASICs can adopt Static Frequency Scaling or power gating which helps reduce power because they allow a chip to run at lower voltages.

Also, ASICs provide the benefits of size and integration where miniaturization is essential to implement wearable devices, which are required to have a small form factor and should not be bulky or imposing in any way [6]. A new ASIC can also incorporate several functions into the same chip, hence enhancing chip efficiency in terms of power and space.

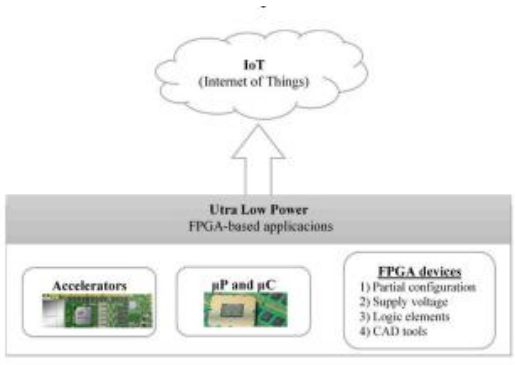

Fig.4: ULP FPGA-based application in IoT [9]

In other words, the integration of custom ASICs in IoT wearables enhances global power regulation as the chips are made especially for certain tasks. Due to the apparent benefits of long battery life, better performance, and reduced dimensions, these have become imperative for today's wearable devices.

V. Ultra-Low Power Modes

Low power modes are appropriate since most IoT wearables incorporate VLSI technology that requires minimal power consumption. These modes allow wearable such as fitness trackers, smartwatches, wearables, and medical devices to cross energy in case of little use or no use at all. Given that wearables are often powered by batteries, and should be designed to run for long periods between charging cycles, integrating ultra-low power modes is essential to maximize battery life.

Wearable devices much time in idle modes or executing background tasks that do not necessarily need the full processing potential of the device. Low power modes are employed to let these devices be able to function at a minimal level of energy by blocking some circuitries from being powered if not necessary [7]. Such an approach is critical for battery longevity and especially useful when constant checking is needed (such as heart rate or steps counter).

Among those features used to achieve ultra-low power modes, one can mention power gating. The second methodology is known as power gating in which power is switched off to idle or inactive parts of the device. For example, during idle time or when the wearable device does not need to engage the user, power gating puts parts of the circuitry including sensors and display, or communication units under sleep mode. This cuts static power or leakage power by far, the power consumed by the transistors regardless of their switching. In this regard, wearables tend to be more effective in saving power during the standby mode than a power supply that is designed to allow power leakage.

Another technique applied to ultra-low power modes is clock gating whereby the clock signal is removed from sections of the device's circuit when those areas are not required. This decreases the dynamic power consumption because the circuitry is stopped from flipping all the time.

Two such ultra-low power modes are described here as being critical for achieving optimal performance and power

consumption characteristics in IoT wearables based on VLSI design concepts [8]. However, the existence of ultra-low power modes guarantees smart wearable applications' functionality for protracted periods and provides users with an uninterrupted and efficient experience.

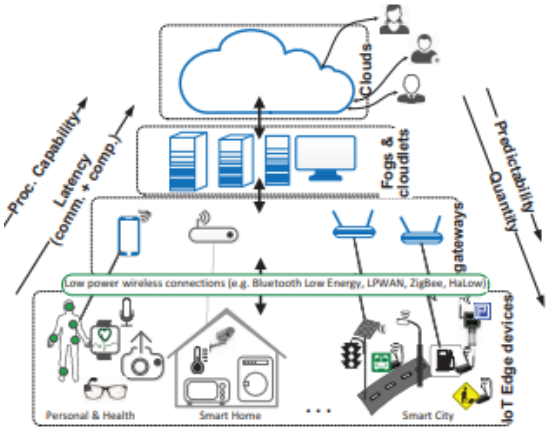

Fig.5: Computation layers in IoT systems and their properties[23]

Concisely, ultra-low power modes are critical to power management in VLSI-based wearable devices because of their ability to reduce power utilization in quiescent mode to achieve longer battery life.

VI. ENERGY HARVESTING TECHNOLOGIES

Energy harvesting can be defined as one of the most significant enabling technologies through which IoT wearable devices minimize their power consumption when this is incorporated into VLSI design. Energy scavenging is the process of extracting and utilizing energy from the immediate environment, or power that is in some way embodied in the surrounding environment and the objects within this, for example thermally, mechanically, or illumination-wise. This capability can act as a complementary power source to the battery decrease the rate at which charging is required and greatly enhance the lifetimes of wearable devices.

In the context of wearables, energy harvesting offers a promising solution to one of the major challenges: In given below points, common applications can be observed in activities ranging from general lighting control and power saving in residential and commercial buildings to power efficiency in devices that suffer from low battery power [9]. Compared to dependent energy, wearables based on naturally available energy can prolong their functioning even under battery power depletion and thus minimize the user's reliance on recharging.

Thermoelectric generation as a form of energy harvesting is achieved by harvesting the heat generated by the wearer of the wearable and converting this to electrical energy. Because wearables are often attached to the skin, this technique enables the device's power to be constantly produced for as long as this is connected to the client. This can be especially important in health monitoring devices, or the need for fitness trackers with long continuous use, as they can use body heat as a consistent energy source.

Another way to harvest energy in wearables is through piezoelectric generation, where electrical power is generated through mechanical movement such as walking, running, and other movements. This is most applicable for fitness devices and smartwatches because this can harvest energy during activity time, so the battery is less or not required for functions required during activity.

Furthermore, light energy collection is employed by integrating tiny solar panels into the wearable technology to collect light, from indoors or outside. This enables the wearables to charge automatically in areas that are well-illuminated, thus maximizing the use of the device.

Efficient energy management can be achieved through an optimized circuit layout for HET wearables integrated into the VLSI design of electronics that require little power conversion loss [10]. This leads to longer battery duration, increased device independence, and convenience for the user.

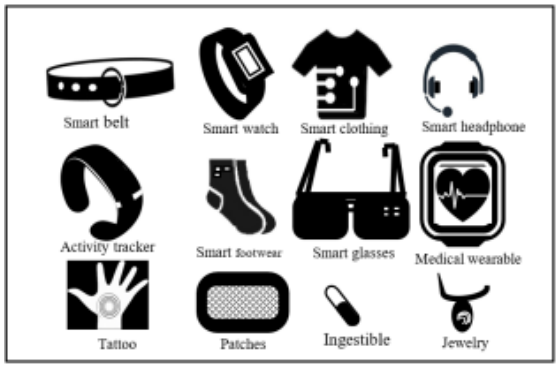

Fig.6: Different wearables developed for various applications.[24]

Altogether, harnessing energy technologies benefits wearables by adding another power source, decreasing charging frequency, enhancing the lifetime of gadgets, and supporting smart and continuous working in healthcare, health, and other IoT-related applications.

VII. System-On-Chip (SoC) Integration

Integration of System-On-Chip (SoC) is a critical task in minimizing energy usage when designing IoT wearables especially if using VLSI (Very Large Scale Integration) technology. SoC which refers to the system on chip refers to a design that is incorporated with the processor, memory, sensor, communication modules, and power management units all in one chip. This integration eliminates the need for almost any terminals so the power lost between functional elements is less, which makes the whole telephone system less power-hungry than similar systems.

As previously constructed, components such as microcontrollers, sensors, memory, and other communication parts are wired together by dedicated buses. These interfaces cause additional, undesirable ratios that arise when the device has ongoing processes that require, for example, regularly measuring a user's health status or transmitting data over a wireless link [11]. Due to the integration of all or most elements on a chip, much of this overhead is eliminated in SoC integration which passes on direct and efficient interaction between functional units.

They also require highly optimized interconnects between each of the SoC design's components. These interconnects are shorter and faster in VLSI design and hence decrease both the dynamic power (used during data processing and communication) and the static power (leakage power). This energy loss saved in inter-component communication is even more relevant in wearables as the devices have to be endowed with low power consumption to continuously monitor and communicate for an extended time

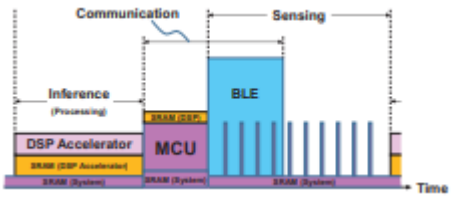

Fig.7: Breakdown of the Current Consumption in SoC [25]

Also, the power distribution in an SoC is highly manageable, making this possible to distribute power in small increments. For instance, this is possible to switch individual components 'on' or 'off' in the course of use to eliminate power wastage. This also supports Dynamic Voltage and Frequency Scaling – SoCs with one or more sections may be powered up in the course of working with different loads.

Besides power saving, integration of more functions into SoC results in a small form factor of wearable devices, and small, lightweight wearables [12]. This is especially true in wearables because such devices should be portable and as non-intrusive as possible.

Thus, the integration of SoC in VLSI-based wearable devices improves the devices' energy absorption capabilities owing to decreased energy loss between the related peripherals, effective power control, and the inherent small and complex nature of SoC-based wearable devices. This leads to increase of batter duration and enhanced performance in wearables devices.

VIII. Power-Efficient Communication Protocols

Energy-conserving communication protocols are crucial in low-power applications in IoT wearable devices fabricated using VLSI technology; especially where such devices entail wireless communication and are energized by small batteries. Smart clothing devices such as smart footwear, wrist wearables like smartwatches, smart rings, smart eyewear, and smart clothing accessories such as health monitors need to have relatively continuous interaction or periodic connectivity with smartphones, the clouds, or other smart systems. One of the most important techniques that need to be integrated into VLSI systems is using low power transfer standards while transferring data.

The low-power connectivity option for wearables most commonly in use is Bluetooth Low Energy (BLE) technology, commonly referred to as BLE. BLE is intended for low-energy applications in which, for example, a watch operates. Unlike normal Bluetooth, BLE has much less energy demand because they communicate in small measures and not constantly in some particular Piconet. This makes it

possible for wearables to send information in between while waiting for the next event so that this can avoid often discharging its battery [13]. Low-duty-cycle operation is also supported by BLE which entails that the device can be kept in substates that consume very little power until data needs to be transmitted; hence less power will be used.

That holds much truth; however, another equally efficient standard for wearable devices is Zigbee, a low power low data rate bus that is best known for its use in short-range wireless networks. Zigbee is most suitable for wearables that function within settings that demand low power usage and feature meshes. This protocol permits multiple sources, which means devices can forward data to other nodes, which means message communication can extend beyond a single distance without burdening a device's battery. Energy consumption is a major factor that affects wearables used for long-term monitoring without frequently changing or recharging batteries, therefore, Zigbee's efficiency is ideal for wearables.

These power-efficient protocols seamlessly integrate with VLSI designs of the communication hardware that are designed for power optimization [14]. Incorporating these protocols into the design of the chip means that wearable devices will be able to reduce power consumption during communication and this is one of the key factors that consumes most energy in IoT devices.

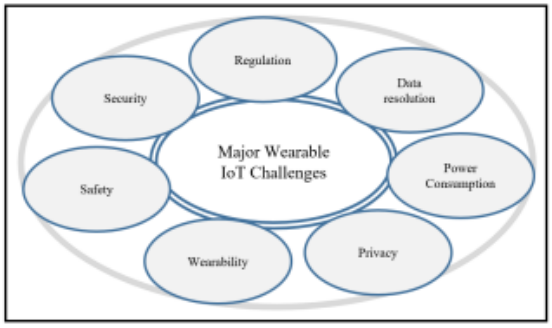

Fig.8: Major challenges of wearable IoT technology.[24]

In conclusion, incorporating power-efficient communication protocols such as BLE and Zigbee into VLSI-based IoT wearables is important for minimizing data transfer energy consumption, hence enabling effective utilization of the limited energy storage in wearable technology to suffice for long-term power requirements in real applications. Wireless protocols can allow such devices to perform wireless communication operations with the least energy consumption possible, thus making them a crucial part of wearable technology devices.

IX. Advanced Semiconductor Processes

Semiconductor process technology advanced in the IoT wearable devices by the use of novel technologies namely; FinFET (Fin Field-Effect Transistor) and the ultra-low power CMOS (Complementary Metal-Oxide-Semiconductor). These processes also allow wearable devices to run at a lower voltage, which is a requirement in keeping most passive wearable devices' power consumption low whilst preserving good performance for devices with limited power resources such as small battery capacities.

One of the most considerable problems in fashioning power-sensitive wearables is leakage current—the current that flows through a transistor when the switch is open. FinFET technology is a 3D transistor structure that solves the above-mentioned problem. In contrast with planar transistors that have a higher leakage current in smaller nodes because of poor control of the gate, FinFET transistors introduce the gate surrounding the "fin" of the transistor channel [15]. This three-dimensional structure offers a much better electrostatic control of the channel with instantaneous leakage currents. This results in less standby power consumption which is important for wearables most of the time spending their time in low power mode or completely idle.

Even lower power ULPCMOS technologies also contribute to power consumption optimization for VLSI-based wearable devices and allow controlling the number of transistors operating at lower voltage levels. Scaling down the supply voltage directly decreases both the dynamic power associated with transistor switching and subthreshold leakage power. The CMOS circuits can employ special low-power transistors which require very low power for switching across, this will keep on reducing the power consumed by the wearable device particularly when consistently monitoring activities for example in a fitness tracking device or a health monitoring one.

The application of these sophisticated methodologies into VLSI designs enables the development of customized

wearables' chips with the highest performance and low power consumption. Both FinFET process and ultra-low power CMOs enable manufacturers to create end products that can power various tasks including sensor data processing, communication, and AI inference power efficiently

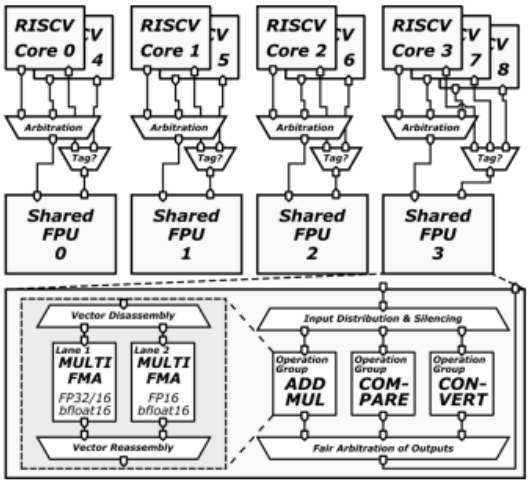

Fig.9: Architecture of the shared multi-precision FPU and its integration in the 9-cores cluster. [26]

Therefore, complex semiconductor processes such as FinFET and ultra-low power CMOS are very important for minimizing the power requirements of IoT wearable device development [16]. These technologies reduce leakage current, lower the operating voltage, and effectively deliver the same performance thus saving power and increasing battery durability.

X.Low-Power Memory Technologies

One of the most critical components of VLSI-based IoT wearables is memory with low power methodology is essential to cut down the total power contingency of such devices especially if this is used for applications that include record keeping including health and fitness. In wearable devices, sensors employ memory for data storage and processing of high volumes of sensor data and this drains power. Specifically, effective principles can be applied, such as NVM technology and the partitioning of memory based on using frequencies that effectively minimize power requirements, thus increasing energy efficiency for wearable devices.

Non-volatile memory (NVM), including Flash, FRAM (Ferroelectric RAM), or MRAM (Magnetoresistive RAM), is the type of memory that requires no power to maintain memory contents when the device is turned off. This characteristic makes NVM highly suitable for wearables because this minimizes power used by repeated memory accesses and storage processes [17]. On the other hand, motion traditional volatile memory for instance SRAM or DRAM always needs power to retain data hence consuming more energy. When incorporated into wearables' VLSI circuits, this becomes possible to store activity, health data, or any other data in small amounts in an effective way but with little power consumption.

The low-power memory design also employs the following technique: memory partitioning based on the usage frequency. In this approach, memory blocks are partitioned and modified based on the usage frequency of the memory. What is frequently accessed is stored in low-power high-speed memory while what is used less frequently is stored in larger slower to access memory which takes less power. This dynamic memory allocation means that more memory access is not made when this is not required and hence saves power needed when, for instance, most wearable devices require this as they periodically wake up from a power-saving mode.

Similarly, when this comes to the architectures of low-power SRAM, well-optimized bit line structures and efficient control of leakage currents can be incorporated to cut the power dissipation during the actual memory operations in wearables, since real-time data processing is so much a crucial factor.

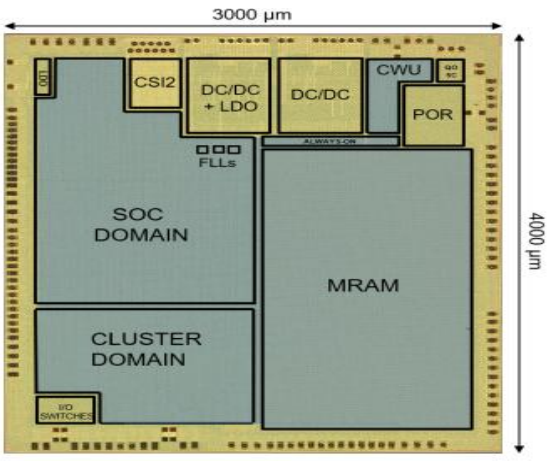

Fig.10: Vega SoC Die Micrograph.[26]

Hence, memory technologies such as NVM and memory partition in low-power IoT optimize power in wearables since they reduce the need to access memory frequently and manage data storage and the life cycle of the device [18]. These technologies form critical components of the efficient power management for memory-bound wearable systems implemented using VLSI technology.

XI. Thermal Management Optimization

Optimization of the thermal load is the key product of power efficiency of IoT wearable devices that are applied to VLSI (Very Large-Scale Integration) technologies. Portable devices are typically small and compact and, as such, integration of multifunctional circuits that are both high-performing and power efficient whilst minimizing the emission of heat is a challenge. The management of heat in VLSI circuits offers protection against heat dissipation, minimizes the use of the cooling processes, and guarantees longer operation of the devices.

When running data from sensors, wirelessly transmitting data, or computing data, the integrated circuits (ICs) behind IoT wearable devices produce heat. Lack of sufficient thermal control results from increased heat levels that impact the part's performance drain the battery or even harm the gadget [19]. These effects are countered in VLSI through efficient thermal management that controls the heat produced at the circuit/die level ensuring that wearables work at safe temperatures. This reduces the need for extra power supply for cooling systems, which is very important for devices with restricted battery capacity.

Another typical practice in the application of VLSI in wearables is the distribution of high and low-power devices on the actual hardware layout over the chip. Also, thermal-aware floor planning is used in VLSI design to allocate components in a way that any point of heat energy density is well controlled to avoid heat build-up. Because the heat is dissipated per area of the chip, the wearables can skip hotspots which are expected to be actively cooled.

Other unique packaging techniques, including the System-In-Package (SiP) and Multi-Chip-Module (MCM) packages, are applied to enhance thermal management. These methods include stacking one chip on another in which several chips can be packaged into a single one under the guise of an efficient manner in which heat produced is dissipated from the crucial parts.

Fig.11: L-IoT approach.[27]

There are also chip-level designs; the power management solutions, such as Dynamic Voltage and Frequency Scaling (DVFS) that can lower the speed and voltage frequency of the device when this is idle reducing the heat that this produces. This not only reduces energy usage as a way of saving energy but also offsets the thermal profile of the wearable.

Therefore, thermal management optimization in the context of VLSI design is vital for heat control, battery conservation, and preservation of the performance and durability of IoT wearables [20]. Through proper management of heat generation in electronics, wearables can sustain the best possible energy output while not getting too hot to require cooling innovations that gobble up batteries.

XII. Conclusion

Reducing power consumption in these IoT Wearable devices using VLSI technology is crucial for their diverse utility, efficiency, and durability. In its use for health monitoring, fitness tracking, and as a medium for entertainment among other uses, wearables are now a necessity that has to be miniaturized, and integrated with long-lasting batteries and high performance. In particular, wearables suffer from the inability to deliver longer battery life because of the amount of data that they require to process, and the availability of VLSI solutions for highly integrated and optimized circuit topologies that facilitate power management to enable the required functionality of the wearable system.

To optimize the power in VLSI on IoT wearables these are the following main approaches: This is the use of low power design methods like reduction in supply voltage, and selection of proper transistor size that are most important for reducing both dynamic and standby power. These techniques allow wearables to run effectively; in situations where power access is constrained and recharging is scarce.

Other advanced power management strategies for DSP, known as Dynamic Power Management (DPM), include Dynamic Voltage and Frequency Scaling (DVFS) that adapt the performance levels to match the real-time processing requirements. This enables wearables to save power during non-consumption or low periods yet deliver high power during the high-consumption period.

There are also ultra-low-power modes that allow for minimizing power consumption over the inactive points of interacting with the application and power gating which is employed in turning off the unused portions of the circuit. application-specific integrated circuits AsICs used selectively inside wearable devices, particularly for wellness tracking or exercising, give much higher effectiveness per power than universal processors.

Using some techniques like energy harvesters like, kinetic energy, body heat, and light energy can also be used as additional powering up techniques other than charging this frequently. This is a potential method of increasing device life and guaranteeing continuous operations.

Furthermore, System-on-Chip (SoC) integration which tends to combine processing, sensing, memory, and communication functionalities into a single chip minimizes inter-communications losses of energy and improves the general performance of the SoC systems. This level of integration contributes to making the wearables both easier to design and more power-efficient to operate.

Smart communication protocols that include Bluetooth Low Energy (BLE) and Zigbee decrease the energy consumption needed to perform the data transmission a requirement for IoT devices that require periodic data updates. In addition, innovative semiconductor processes of FinFET and ultra-low power CMOS technologies decrease leakage currents and permit low voltage drives, lowering energy issues at the hardware system level.

Finally, using low-lethality memory technologies such as NVM and different memory partitioning depending on usage helps in preventing most transformations that make frequent memory use and therefore, the memory part of the health data logging power hungry.

Therefore, power minimization in IoT wearable devices through the use of VLSI is a multilayered process that requires the functions of several design methods that range from memory optimization to communication style and energy scavenging. These developments are crucial for resolving the power issues of wearables and guaranteeing the devices can deliver the performance necessary while being power economical and thereby increasing the battery life expectantly, thus adjusting the user experience. Through the implementation of these featured VLSI design methodologies, IoT wearables are likely to be made sustainable, dependable, and feasible for use.

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